MRAM HAVING ERROR CORRECTION CODE CIRCUITRY AND METHOD THEREFOR

Abstract of the Disclosure

An embedded memory system (10) uses an MRAM core (12) and error correction code (ECC) corrector circuitry (20). The ECC corrector circuitry identifies soft memory bit errors which are errors primarily resulting from an MRAM bit not being correctly programmed. The errors are identified and corrected during a read or a write cycle and not necessarily when the memory is in a special test mode. As errors are corrected, the error corrections are counted by an error counter (24) to create a count value. The count value is stored in the MRAM core itself and can later be retrieved and read during a test mode for an indication of how many bit corrections are required for the MRAM core over a period of time. The count value is stored by using an unused portion of a write memory cycle during a read operation.